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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) BUR920040112US1(17618)	
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		First Named Inventor Anil K. Chinthakindi	
		Art Unit 2822	Examiner Tsz K. Chiu
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s).</p> <p>Note: No more than five (5) pages may be provided.</p>			
<p>I am the</p> <p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>39,394</u></p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____</p>		 <p>Signature</p> <p><u>Leslie S. Szivos, Ph.D.</u></p> <p>Typed or printed name</p> <p><u>516-742-4343</u></p> <p>Telephone number</p> <p><u>May 29, 2007</u></p> <p>Date</p>	
<p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p>			

*Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants: Anil K. Chinthakindi, et al. **Docket:** BUR920040112US1 (17618)
Serial No.: 10/710,847 **Examiner:** Tsz K. Chiu
Filed: August 6, 2004 **Art Unit:** 2822
For: FEOL/MEOL METAL
RESISTOR FOR HIGH END
CMOS
Confirm. No.: 6756

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REASONS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

The following Arguments are being submitted in support of Appellants' Pre-Appeal Brief Request for Request for Review.

CERTIFICATION OF ELECTRONIC FILING

I hereby certify that correspondence is being deposited with the United States Patent & Trademark Office via Electronic Filing through the United States Patent and Trademark Office e-business website, on May 29, 2007.

Dated: May 29, 2007



Leslie S. Szivos, Ph.D.

Claims 1 – 10 are pending in this application. In an Office Action dated March 13, 2007, the Examiner issued a final rejection of all of these claims over U.S. Patent No. 6,586,311 to Wu (hereafter “Wu”), U.S. Patent No. 6,777,752 to Osanai et al. (hereafter “Osanai”), and U.S. Patent No. 5,554,873 to Erdeljac et al. (hereafter “Erdeljac”). Specifically, Claims 1-3, 5-8 and 10 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by Wu. Claim 4 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Wu and Osanai. Claim 9 stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Wu and Erdeljac.

In this application, Claim 1 is an independent claim. Claims 2, 3, 5, 6, 8, 9, and 10 depend from Claim 1. Claim 4 depends from Claim 3. Claim 7 depends from Claim 6.

I. CLEAR ERROR

The rejections of the claims are improper because the combined disclosures of Wu, Osanai, and Erdeljac do not disclose or suggest a metal resistor located on, or in close proximity to, a surface of a semiconductor substrate, said metal resistor comprising at least a conductive metal; and a first level of metallization above said at least one metal resistor.

II. DISCUSSION

A. This invention

The present invention relates to at least one metal resistor comprising a conductive metal as disclosed and claimed in Claim 1. Further, a first level of metallization is provided above the at least one metal resistor

B. Wu

1. Wu does not disclose a metal resistor

Wu discloses a *semiconductor resistor* formed within a semiconductor substrate below the top surface of the semiconductor substrate.

In the Office Action dated January 26, 2007, the Examiner alleged that Wu discloses “at least a conductive metal” and refers to element 430 in FIG. 8 of Wu. Appellants submit that element 430 is an undoped polysilicon layer, as disclosed in column 5, lines 5 – 8 in Wu, which states “As shown in FIG. 4, an undoped polysilicon layer 430 may form a portion of a structure layer 420 such as an epitaxial semiconducting layer.” An undoped polysilicon layer is not considered a conductive *metal* by one of ordinary skill in the art.

In the Examiner’s response with respect to Claim 1, the Examiner alleges that there is at least one metal resistor in FIG. 8 of Wu. Appellants submit that no metal resistor is present in Figure 8 of Wu, let alone in any of the other figures in Wu, or in any of the disclosure of Wu. The absence of any metal resistor in Wu is herein demonstrated in various ways.

First, examination of the elements that the Examiner alleges to be a metal resistor shows that none of them are metal resistors. In the Examiner’s response with respect to Claim 2, the Examiner alleges that elements 640 and 540 are the at least one metal resistor. Examination of the specific reference numerals 640 and 540 in Wu shows that element 640 is a dielectric. Wu does not describe reference numeral 540 in the specification. Based on FIGS. 7, 9, and 10, however, one of ordinary skill in the art may assume that reference numeral 540 refers to element 640, or at least comprises the same material as element 640. In either case, the element referred to by 540 would be an oxide. Therefore, *element 540 cannot be a metal resistor.*

Second, all the references to the term, “resistor,” in Wu are general statements, and do not have any associated reference numerals. References to “a resistor,” “the resistor,” and “a passive resistor” refer to a layer of polysilicon. A polysilicon resistor is not a metal resistor since polysilicon is not metal. Therefore, *none of the terms in Wu containing “resistor” refer to a metal resistor.*

Third, a text search of Wu for the term, “metal,” shows that occurrences of that word are found only within the context of a metal oxide semiconductor field effect transistor (MOSFET or MOS transistor) or within the context of a metal layer. Examination of FIG. 2 and FIG. 7 shows that the metal layer refers to a blanket cobalt metal layer. A blanket metal layer may not be considered a resistor by one of ordinary skill in the art. Therefore, *no references including the word, “metal,” in Wu actually refer to a metal resistor.*

Wu provides a method of fabricating a semiconductor structure in which a salicide block mask prevents the formation of silicide on a portion of the silicon substrate.

2. Wu does not provide a first metallization level atop the metal resistor

Appellants further note that Wu does not disclose a first metallization level atop the metal resistor, as presently claimed. A metallization level, as is well known to those skilled in the art, represents a dielectric material that has conductive features (conductive vias and/or lines) embedded therein. Structures obtained out of the metal layer 700 in Wu are not metallization, as it is referred to in the industry or in the present application.

C. Osanai and Erdeljac

While Osanai discloses a polycrystalline silicon resistor, it does not disclose a metal resistor or a first metallization level atop the metal resistor, as presently claimed. Erdeljac is further removed than Osanai et al., since it is directed to polysilicon resistors, not metal resistors, as presently claimed.

D. Difference between the claims of the present application and Wu, Osanai, and Erdeljac

1. Wu, Osanai, and Erdeljac do not disclose a metal resistor, while the claims of the instant application positively recite a metal resistor.
2. Wu, Osanai, and Erdeljac do not provide a first metallization level atop a metal resistor, while the claims of the instant application specifically recite the presence of a first metallization layer.

III. CONCLUSION

Because of the above discussed differences between Claim 1 and Wu, as well as the combined disclosures of Wu, Osanai, and Erdeljac, the claims of the instant application are not anticipated or rendered obvious by Wu or the combined disclosures of Wu, Osanai, and Erdeljac. Thus, the rejections of the claims over Wu, Osanai, and Erdeljac are not proper. If the panel believes that a telephone conference with the Appellants' Agents would be advantageous to the disposition of this case, the panel is requested to telephone the undersigned.

Respectfully submitted,



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